CLAIMS:

1. Pipeline synchronisation device for transferring data between clocked devices (WD, RD) having different clock frequencies (CLK), comprising

a mousetrap buffer (MT, MT1, MT2) for exchanging data (Wdat, Rdat) with one of said external devices (WD, RD), said mousetrap buffer (MT, MT1, MT2) having a signalling output (Wack, Rreq) for coordinating the data exchange with the external device (WD, RD),

characterised by

a synchroniser (S1, S2) adapted to synchronising the change in a signalling output (Wack, Rreq) with the clock (CLK) of the external device (WD, RD).

2. Pipeline synchronisation device according to claim 1, wherein the synchroniser (S1) is adapted to synchronising the change in the signalling output (Wack, Rreq) with a high phase or a low phase of the clock (CLK) of the external device (WD, RD).

3. Pipeline synchronisation device according to claim 2, wherein the synchroniser (S1) is adapted to delaying a transfer of a change in the signalling output (Wack, Rreq) until the clock (CLK) of the external device (WD, RD) is either high or low.

4. Pipeline synchronisation device according to claim 3, wherein the synchroniser (S1) comprises a synchronising latch (L) having a synchronising input (SI) for receiving the signalling output (Wack, Rreq), a synchronising output (SO) for outputting the received signalling output (Wack, Rreq) to the external device (WD, RD) and a control input (e) for enabling the output of the received signalling output (Wack, Rreq) to the external device (WD, RD).

5. Pipeline synchronisation device according to claim 4, wherein the synchroniser (S1) comprises an EXNOR-gate (50) having two inputs and one output, the inputs of the EXNOR-gate (50) being connected to the synchronising input (SI) and output of the synchronising latch (L), and the synchroniser (S1) comprises a wait-component

(Wait4) having an input (d) connected to the output of the EXNOR-gate (50), an input connected to the clock (CLK) of the external device (WD, RD) and an output connected to the control input (e) of the synchronising latch (L).

6. Pipeline synchronisation device according to claim 5, wherein the wait-component (Wait4) is adapted to outputting a change from low to high in the input (d) only, if the clock (CLK) of the external device (WD, RD) is high, and outputting a change from high to low in the input (d) irrespective of the state of the clock (CLK) of the external device (WD, RD).

7. Pipeline synchronisation device according to claim 6, wherein the wait-component (Wait4) comprises an inverter (65) and an arbiter (60) having an input for receiving the inverted clock signal (CLK), which is inverted by the inverter (65), and an input (d) for receiving the output of the EXNOR-gate (50) and an output for transmitting the input (d).

8. Pipeline synchronisation device according to claim 1, wherein the synchroniser (S2) is adapted to synchronising the change in the signalling output (Wack, Rreq) with a rising and/or a falling edge of the clock (CLK) of the external device (WD, RD).

9. Pipeline synchronisation device according to claim 8, wherein the synchroniser (S2) comprises two synchroniser (S1) according to claim 3, which are adapted to delaying a transfer of a change in the signalling output (Wack, Rreq) until the clock (CLK) of the external device (WD, RD) is either high or low, wherein a first of the two synchronisers (S1) is adapted to transferring a change in the signalling output (Wack, Rreq) of a first mousetrap buffer (MT1) to the external device (WD, RD) and wherein a second of the two synchronisers (S1) receives an inverted clock (CLK) of the external device (WD, RD) and is adapted to transferring the signalling output of a second mousetrap (MT2) to the first mousetrap buffer (MT1).

10. Pipeline synchronisation device according to claim 8, wherein the synchroniser (S2) comprises an edge synchroniser (UE4) having two wait-components (Wait4) according to claim 6, each being adapted to outputting a change from low to high in the input (d) only, if a received clock is high, and outputting a change from high to low in the

input (d) irrespective of the state of the received clock, wherein a first of the two wait-components (wait4) is adapted to receiving the clock of the external device (WD, RD) and outputting a change in its input (ar) to the external device and wherein a second of the two wait components (wait4) is adapted to receiving an inverted clock (CLK) from the external device (WD, RD) and outputting a change in its input (d) to the input (ar) of the first wait component (wait4).

11. Pipeline synchronisation device according to claim 10, wherein the synchroniser (S2) comprises a synchronising latch (L) having a synchronising input (SI) for receiving the signalling output (Wack, Rreq), a synchronising output (SO) for outputting the received signalling output (Wack, Rreq) to the external device (WD, RD) and a control input (e) for enabling the output of the received signalling output (Wack, Rreq) to the external device (WD, RD).

12. Pipeline synchronisation device according to claim 11, wherein the synchroniser (S2) comprises an EXNOR-gate (50) having two inputs and one output, the inputs of the EXNOR-gate (50) being connected to the synchronising input (SI) and output (SO) of the synchronising latch (L), and the synchroniser (S2) comprises an edge synchroniser (UE4) having an input (d) connected to the output of the EXNOR-gate (50), an input connected to the clock (CLK) of the external device (WD, RD) and an output connected to the control input (e) of the synchronising latch (L).

13. Pipeline synchronisation device according to claim 1, wherein the mousetrap buffer (MT1) is adapted to receiving data (Wdat) from the external device (WD) and the mousetrap buffer has a signalling output (Wack) for acknowledging the receipt of data to the external device (WD).

14. Pipeline synchronisation device according to claim 1, wherein the mousetrap buffer (MT2) is adapted to transferring data (Rdat) to the external device (RD) and the mousetrap buffer has a signalling output (Rreq) for requesting the transfer of data to the external device (RD).

15. Pipeline synchronisation device according to claim 13, wherein the mousetrap buffer (MT1) comprises an EXOR-gate for receiving a read request signal (Rreq) from the

mousetrap buffer (MT1) and a read acknowledge signal (Rack), a latch (L) having a control input (e) for enabling and disabling the receiving and transferring of data, wherein the synchroniser is adapted to synchronising an output (d) of the EXOR-gate with the clock (CLK) of the external device (WD) and to supply the synchronised output (d) to the control input (e) of the latch (L).

16. Pipeline synchronisation device according to claim 15, wherein the synchroniser (S2) is adapted to synchronising the change in the output (d) of the EXOR-gate with a rising and/or a falling edge of the clock (CLK) of the external device (WD).

17. Method for transferring data between clocked devices having different clock frequencies (CLK), comprising the steps of

using a mousetrap buffer for exchanging data (Wdat, Rdat) with one of said external devices (WD, RD), wherein said mousetrap buffer (MT, MT1, MT2) outputs a signal (Wack, Rreq) for coordinating the data exchange with the external device characterised by the step of

synchronising the change in the output signal (Wack, Rreq) with the clock (CLK) of the external device (WD, RD).